

GALS DESIGNS IMPLEMENTATION ON “STRUCTURED ASIC” PLATFORMS

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Abstract: *Large and complex digital circuits require new modular architectures that allow power consumption reduction and integration of various building block modules with different requirements regarding the clock frequency. The paper evaluates the possibilities of implementing asynchronous circuitry specific to GALS (Globally Asynchronous Locally Synchronous) architectures on “structured ASIC” (Application Specific Integrated Circuit) platforms to create a new class of digital circuits that can address the issues of large circuit design.*

Key words: *GALS, asynchronous, SOC, structured ASIC.*

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